REMARKS

In accord with the Restriction Requirement, Applicant elects the species of claims 8-13 and 30-37. Applicant has withdrawn the other claims without prejudice.

Applicant includes herewith amended drawings in accord with the statements of the Examiner to remove the objection thereto.

Applicant has made the amendments to the specification required by the Examiner to remove the objection thereto.

Applicant has made appropriate claim amendments as suggested by the Examiner in conjunction with additional claim amendments that are believed to remove the outstanding objections to the claims.

Claims 8-13 and 30-37 stand rejected under 35 USC 112 as being indefinite for various reasons as discussed below.

The Office Action states that the term "standard glitch" is unclear. Although Applicant believes that the term "standard glitch" is defined very specifically in the specification so that one of skill in the art will understand its meaning, which is all that is required for satisfaction of 35 USC 112, nonetheless Applicant has removed that language from the claims because the term is believed to be more specific than is required in light of the cited prior art.

The Office Action states that the term "balanced gates" is unclear in claim 10. It is also stated that the term "gates" is unclear as a type of "delay circuit" because Fig. 6 shows inverters as the delay circuits. Accordingly, Applicant has clarified that "balanced" refers to a rise time and fall time of an input to output pulse response. Additionally, Applicant has removed the term "delay circuit" and replaced it with "logic elements."

The Office Action states that the phrase "providing a delay in the gate" in claim 30 is unclear. Although Applicant removed the term for claim 30, Applicant has substituted the phrase "pulse propagation delay" for "delay" where appropriate in other amended claims, e.g., claim 8.

With respect to claims 31 and 32, the Office Action appears to indicate there is no basis

in the specification to claim adjusting the length or channel characteristics of FETs of gate circuits. However, Applicant refers the Examiner to the chart on page 11 which shows that the gates may be adjusted as desired. For instance, the channel width of FET M5 in FIG. 6 appears to have been significantly altered as compared to FET M5 in FIG. 1. Please note that the specific example of FIG. 6 is intended only as an example of a presently preferred embodiment of the invention. Please note further that M5, M6, M7, and M8 act in coordination with each other and that the example discusses only the occurance of a glitch at node 134 which node is clearly part of a feedback loop circuit configuration. Moreover, to attempt show all possible variations of the present invention is impractical. Instead, Applicant provides more than sufficient information and examples of use the invention so that one of skill in the art can apply the invention to any particular type of component of interest.

The Office Action states that "the channel" in claims 33 and 34 is indefinite because it is unclear which channels are involved. Accordingly, Applicant has clarified by distinguishing a first channel from a second channel in claim 31, from which claims 33 and 34 depend.

The Office Action states that the term L3 is not understood in claim 37. Applicant has significantly changed claim 37 so that the term is no longer used in claim 37. However, Applicant now uses the terms L1, L2, and L3 in other claims in a manner that is believed to be clear. L1, L2, and L3 are defined as pulse widths. FIG. 4 provides an excellent example of input pulses of different input pulse widths catergorized as less than a pulsewidth L1, greater than pulse width L1 but less than pulse width L2, and greater than pulse width L3 and the resulting selectively modified output pulse widths in accord with the invention. For instance looking at FIG 4., it could be said that an input glitch 412 having a pulse width less than a selected design pulse width L1 as per the language of claim 30, would exit the circuit as pulse 418 so dimenished that it is not capable of causing a subsequent gate to change states.

The Office Action states that the terms "time constant" "threshold" and "would" are unclear. Applicant has amended the claims to state whether or not the glitch (or signal pulse) is able to trigger a change in the logic state of a subsequent logic circuit. This is believed to clarify what Applicant intended. Applicant has removed the word "would" from the claims but respectfully submits that use of the term "would" is not inherently unclear.

Other amendments have been made to the claims that are believed to remove any other remaining grounds for this rejection.

In light of the amendments and the comments above explaining the amendments, it is respectfully submitted that the rejection under 35 USC 112 is traversed.

Claims 8-13, and 30 - 31 stand rejected under 35 U.S.C. 102(b) as being anticipated by Bansal (SUP 5,504,703).

Although other limitations are added to claim 8, some of which have already been discussed above, Applicant has effectively amended claim 8 to include the limitations of claim 9. Claim 9 is cancelled. Amended claim 30 now also includes limitations somewhat similar to those of claim 9. Accordingly, the outstanding rejection to claim 9 is now discussed.

Claim 9 stands rejected because, as best understood, Bansal does not specifically say whether or not the delay is different (or spread equally) as between the logic gate and the inverters in the feedback path as per the previous claim language. Applicant agrees with the Examiner that Bansal does not specifically disclose this claimed feature. In fact, Bansal is actually fairly clear that the seu hardening components, i.e., the inverters, are inserted without other changes to the existing circuits (see for example Col. 2, lines 43-46 of Bansal).

It is respectfully submitted that a rejection under 35 U.S.C. §102 must contain every element recited in the claim in as complete detail as is contained in the claim and arranged as recited in the claim. M.P.E.P. § 2131. Because it is agreed that Bansal plainly does not contain every element in as complete detail as is contained in amended claims 8 and 30, Applicant respectfully submits that the rejection to amended claims 8 and 30, and their dependent claims, is accordingly traversed.

Any additional amendments made were not necessary to overcome the cited prior art.

Conclusion

It is submitted in view of these remarks that all grounds for rejection have been removed by the foregoing amendments and discussion. Reconsideration and allowance of this application are therefore earnestly solicited.

The Examiner is invited to phone Mr. James M. Cate, attorney for Applicant, 281-483-1001, if in his opinion such a phone call would serve to expedite the prosecution of subject patent application.

Respectfully submitted,

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By _____

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